HIGH EFFICIENCY FREE RUNNING CLASS F OSCILLATOR

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ABSTRACT

A free running 1.6 GHz oscillator yielding 67 % power efficiency with 24 dBm output power is proposed. It is based on the use of a transistor working in the an high efficiency class F associated to an appropriate feedback network. The transistor is a 2 mm gate periphery, 0.7 µm gate length MESFET and it is built by THOMSON foundry. The main impact of the characteristics of the constitutive components on the overall oscillator performance is also discussed.

INTRODUCTION

Both satellite communication systems and new generations of mobile communication systems must meet a number of requirements among which are : high efficiency and reduced size and weight. As an example, the reduction in weight and size of hand mobile telephones is one of the major preoccupation. As a consequence, small size battery cells must be used and low voltage operation capability of amplifiers and oscillators is required. The emergence of high efficiency class F amplifiers, which reveal to be suitable for such application has recently been demonstrated [1], [2],[3],[4],(5].

In fact, class F operation may be seen as the result of the combination of an optimized class AB operation mode (seeing at fundamental frequency) in addition with an appropriate control of harmonic terminations (c/c à $2\omega_0$ and o/c at $3\omega_0$) to obtain a quasi-square wave drain voltage. Such bias conditions of microwave power amplifiers provide reasonnable small signal power gain.

That makes this technique very attractive for use in self-sustained high efficiency power oscillators for which class B and C can't be envisaged, since self-starting conditions cannot be obtained at low level. The application of the class F-technique for the design an build of an 1.6 GHz oscillator is proposed in this paper.

A comparative analysis, in terms of power added efficiency, between amplifier and oscillator configurations is also quantified.

I) - PRELIMINARLY CONSIDERATIONS ON THE EFFICIENCY OF THE OSCILLATORS

Figure 1 shows a conventionnal block diagram of an oscillator.

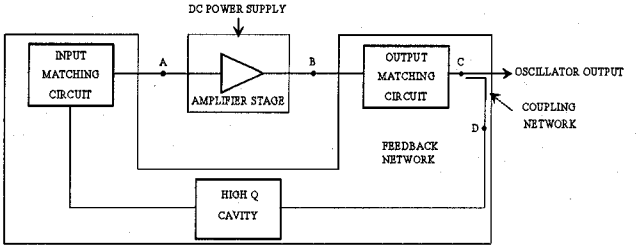

Figure 1 : block diagram of an oscillator

Let us define :

Pin, Pout the input and the output power of the amplifier stage (between (A) and(B)).

Go : power gain of the amplifier stage.

C^2 : coupling factor (between C and D).

α_{out} : output losses (between B and C).

α_f : feedback losses (between D and A).

PDc : DC power consumption.

Posc : available output power of the oscillator.

One can write the following relation ships :

$$Pout = Go\ Pin \quad with \quad Pin = \alpha_{out} \cdot C^2 \cdot \alpha_f \cdot Pout$$

$$Posc = (1 - C^2)\ \alpha_{out}\ Pout = (1 - C^2)\ \alpha_{out} \cdot Go\ Pin$$

$$Posc = (1 - C^2)\ \alpha_{out}^2\ Go\ C^2\ \alpha_f\ Pout$$

The efficiency of the oscillator is

$$\eta_{osc} = \frac{Posc}{Pdc} = (1 - C^2)\ \alpha_{out}^2\ Go\ C^2\ \alpha_f \cdot \frac{Pout}{Pdc}$$

while the power added efficiency of transistor alone used in a class F amplifier configuration is:

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$$\eta_{add\ AMP} = \frac{Pout - Pin}{PDc} = \frac{Pout\ (1 - \alpha_{out}.\alpha_f.C^2)}{PDc}$$

Therefore

$$\eta_{osc} = \eta_{add\ AMP} \cdot \frac{(1 - C^2)\ \alpha_{out}{}^2.Go.C^2.\alpha_f}{1 - \alpha_{out}\alpha_f.C^2}$$

As we have : $C^2.\alpha_{out}.\alpha_f.Go = 1$

$$\eta_{osc} = \eta_{add\ AMP} \frac{\alpha_{out}.Go.\alpha_f - 1}{\alpha_f\ (Go - 1)}$$

Assuming Go >> 1

$$\eta_{osc} = \eta_{add\ AMP} \left(\alpha_{out} - \frac{1}{\alpha_f\ Go} \right)$$

This relationship is very informative ; and leads to the main following key points to design high efficient oscillators :

- first at all , obviously, the power added efficiency of the amplifier must be optimized.
- As far as the power gain Go of the amplifier stage is sufficient, the feedback network losses α_f don't appear as a critical parameter. Therefore high Q cavity can be used to improve phase noise performances.

Following the same argument a lossy monolithic input matching circuit of the amplifier can be implemented without affecting significantly the oscillator performances.

- On the other hand, the output losses α_{out} are of highest importance. In any case this parameter must be minimized and an hybrid MIC is strongly recommended.

II) - THE PROPOSED HIGH EFFICIENCY CLASS F OSCILLATOR

The power amplifier selected to realize the oscillator is a class F single stage MESFET amplifier[6].

A recent publication [7] is fully dedicated to the design of this amplifier.

For our application a 2000 µm gate periphery FET (THOMSON HP07) is used and biased at : V_{gso} = -4.9 V V_{DSO} = 5.5 V I_{DSO} = 12 mA.

The I/V characteristics of the transistor, simulated voltage and current waveforms at the maximum power added efficiency point and the associated load-line is shown in figure 2. and 3.

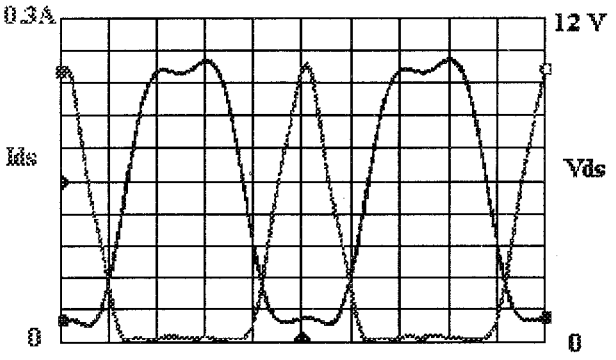

Figure 2 : Current and voltage waveforms

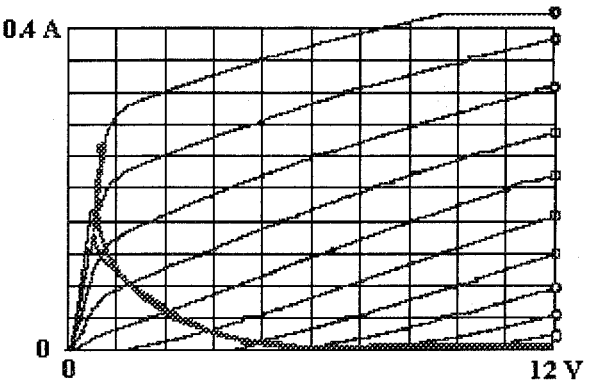

Figure 3 : Associated class F load line

The amplifier has been designed and built and its measured power characteristics at 1.6 GHz are given in figure 4. Its photography is schown in figure 5

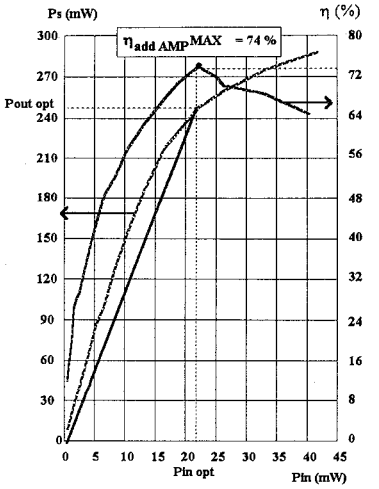

Figure 4 : Measured power characteristics

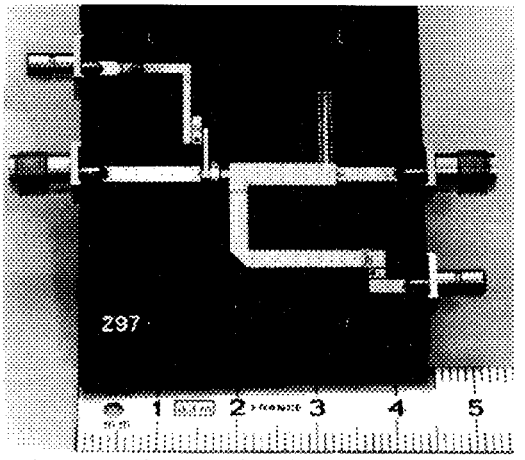

Figure 5 : photography of the amplifier

The slope of the straight bold line superimposed to curves in figure 4 represents the losses of the whole feedback network including output coupling which is necessary to connect to the amplifier stage in order to achieve an optimized high efficiency oscillator.

The block diagram of the corresponding oscillator is given figure 6

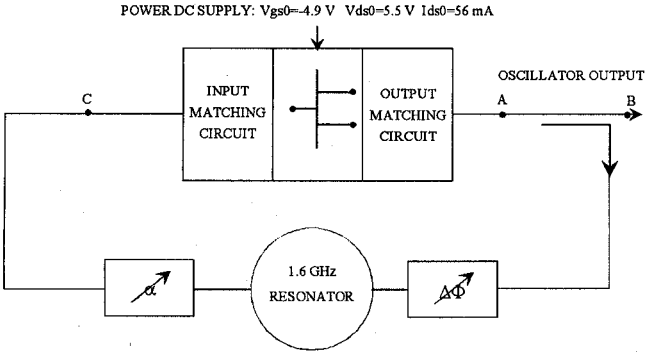

Figure 6: block diagram of the built oscillator

Output losses (between A and B) have been minimized (0.8 dB).

The attenuation of the whole feedback loop (coupler, phase shifter, resonnator, attenuator) has been adjusted to 10.5 dB (slope of the straight line figure 4).

In such conditions the measured power of the osicllator (Point B) is :

$Posc_{dBm}$ = 10 log (Pout) -0.8 dB.

And the measured efficiency has been found to be:

$$\eta_{osc} = \frac{10^{\frac{Posc}{10}}\ \text{dBm}}{V_{DSO} \cdot I_{DSO}} = 67\ \%.$$

with V_{DSO} = 5.5 V and I_{DSO} = 56 mA.

CONCLUSION

A design method of high efficiency power oscillators operating in class F mode has been presented.

Such a technique yields the best achievable efficiency at microwave frequencies for self-sustained free running power oscillators. More than 65 % power efficiency has been obtained. To our knowledge these are the best results published at microwave frequencies.

The possibility of designing such high efficiency oscillators, operating at low bias level is particulary very interesting for mobile communication application.

First phase noise measurements of our built-in oscillator give -90 dBc/Hz at 10 KHz from the carrier and more precise results will be given in the presentation.

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